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09/837,760	04/17/2001	Michael Propp	0382/1D761	8903

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EXAMINER	
AHN, SAM K	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 11/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/837,760	Applicant(s) PROPP ET AL.	
	Examiner Sam K. Ahn	Art Unit 2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-9 and 11-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-8,11-16 and 19-21* is/are rejected.

7)☒ Claim(s) *9,17,18,22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Drawings

2. The drawings were received on 01/24/05. These drawings are acceptable.

Allowable Subject Matter

3. The indicated allowability of claims 9,11,17,18 and 20 is withdrawn in view of the newly discovered reference(s) to Buchanan et al. USP 6,650,661 B1 (Buchanan). Rejections based on the newly cited reference(s) follow.

Claim Objections

4. Claims 4-9 and 11-23 are objected to because of the following informalities:

In claim 4, line 3, "a control" should be "the control", line 5, delete "the control input of", lines 6,8,9 and 10, "an output" should be "the at least one output".

In claim 5, line 2, "an output" should be "the at least one output".

In claim 6, line 2, "an output" should be "the at least one output".

In claim 11, line 2, "outputs together" should be "outputs of the second delay device together".

In claim 22, line 9, "an output" should be "at least one output", line 11, "the output" should be "the at least one output" and line 17, "an output" should be "the at least one output".

Claims 7,12-21 and 23 directly or indirectly depend on claim 4 or 22. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4-6,8,11-14 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saeki USP 6,275,547 B1 (cited previously) in view of McDermott et al. USP 5,926,053 (McDermott, cited previously) and Buchanan et al. USP 6,650,661 B1 (Buchanan).

Regarding claim 4, Saeki teaches (see Fig.1) a first delay device (101,102), a second delay device (105), and a sampling signal line coupled to, and configured to provide a sampling signal (extracted clock) based on an output of the first delay device (101,102), and a sampling device (106) coupled to an output of the second delay device (105) and coupled to the sampling signal line, the sampling device configured to sample the output of the second delay device based on a

value of the sampling signal. However, Saeki does not explicitly teach the first and second delay device having a control input and a control signal line coupled to provide a control signal to, the control input of the first and second delay device, the control signal being based on an output of the first delay device and on a clock.

McDermott teaches (see Fig.4) a first (308) and second (307) delay device including a control input (to receive ADJ1, ADJ2), and a control signal line (from Control Logic,306 coupling to the delay devices) configured to provide a control signal (ADJ1, ADJ2) to, the control input of the first and second delay device, the control signal being based on an output of the first delay device (DLY2 feeding Control Logic) and on a clock (CLK).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to modify Saeki's system to include the teaching of McDermott to include the control inputs in the delay devices and further including the Control Logic to provide the control signal to the delay devices for the purpose of increasing the system performance by including a function of controlling the duration of delay line.

However, Saeki in view of McDermott do not explicitly teach wherein the second delay device includes multiple outputs, and the sampling device is coupled to the multiple outputs.

Buchanan teaches a delay device (24 in Figs.5 and 6) including multiple outputs, and a sampling device (26) is coupled to the multiple outputs (note col.8, lines

13-16). Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Buchanan with the system of Saeki in view of McDermott by using the delay device of Buchanan in the delay device of Saeki (105 in Fig.3A) for the purpose of increasing the speed of transmission between two elements using plurality of lines as compared to a single line. In this case, by using multiple lines between the delay device and the sampling device, one skilled in the art would analyze that the multiple lines provide a higher transmission rate.

Regarding claims 5 and 6, Saeki in view of McDermott and Buchanan teach all subject matter claimed, as applied to claim 4. McDermott further teaches a comparator (310,311 in Fig.6) that includes a first input coupled to an output of the first delay device (receiving DLY2), a second input coupled to the clock (CLK), and an output coupled to the control signal line (from Control Logic,306 coupling to the delay devices), providing an error signal (INC, DEC) between the output of the first delay device and the clock.

Regarding claim 8, Saeki in view of McDermott and Buchanan teach all subject matter claimed, as applied to claim 4. Saeki further teaches wherein the first delay device (101,102) includes multiple outputs (A,B), the sampling signal line (outputting 110) is coupled to the multiple outputs, and the sampling signal is based on the multiple outputs.

Regarding claim 11, Saeki in view of McDermott and Buchanan teach all subject matter claimed, as applied to claim 4. Saeki further teaches wherein the sampling device comprises a latch (106 in Fig.1) configured to sample the multiple outputs together based on the value of the sampling signal (extracted clock).

Regarding claim 12, Saeki in view of McDermott and Buchanan teach all subject matter claimed, as applied to claim 4. Saeki further teaches wherein the sampling device comprises a latch (106).

Regarding claims 13 and 14, Saeki in view of McDermott and Buchanan teach all subject matter claimed, as applied to claim 4. Saeki and McDermott further teach wherein the first and second delay device comprises a first and second delay line, respectively.

Regarding claims 19-21, Saeki in view of McDermott and Buchanan teach all subject matter claimed, as applied to claim 4 or 14. Buchanan further teaches wherein the second delay line comprises an input configured to be coupled to a data source (R1) and is configured to hold data representing one bit of the data source (bit 00 ~ bit 39, note col.8, line 54). And as the bits are received (from

DATA IN, Fig.6, each bit is shifted from bit 00 towards bit 39, and is sampled each time by 40, thus sampling multiple times for each bit, note 12, line 42-45)

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saeki USP 6,275,547 B1 (cited previously) in view of McDermott et al. USP 5,926,053 (McDermott, cited previously) and Buchanan et al. USP 6,650,661 B1 (Buchanan) and in further view of Cranford, Jr. et al. USP 6,721,379 B1 (Cranford).

   Regarding claim 7, Saeki in view of McDermott and Buchanan teach all subject matter claimed, as applied to claim 4. McDermott further teaches adjustment device disposed between the output of the comparator and the control signal line, and configured to provide the control signal (ADJ1, ADJ2) on the control signal line based on the error signal (INC, DEC). However, McDermott does not explicitly teach wherein the adjustment device is a voltage adjustment device. Cranford teaches (see Fig.2) a voltage adjustment device (22''' charge pump) receiving error signal (UP, DW), and adjusting the control signal (Control Voltage, CIN) delivered to delay devices (22',26). Therefore, it would have been obvious to one skilled in the art at the time of the invention to modify McDermott's system to include Cranford's charge pump receiving error signals as it is well-known in the art to implement the charge pump coupled to a comparator.

7. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saeki USP 6,275,547 B1 (cited previously) in view of McDermott et al. USP

5,926,053 (McDermott, cited previously) and Buchanan et al. USP 6,650,661 B1 (Buchanan) and in further view of Eitan (cited previously).

Regarding claims 15 and 16, Saeki in view of McDermott and Buchanan teach all subject matter claimed, as applied to claim 13. Although Saeki teaches an inverter in the first delay line (15) and further suggests that a ring oscillator may be combined with delay circuit (note col.11, lines 9-11), Saeki in view of McDermott and Buchanan do not explicitly teach wherein the first delay line includes cascaded inverters including an odd number of inverters.

Eitan teaches (see Fig.1) cascaded inverters including an odd number of inverters (30, note col.1, lines 13-27) forming a ring oscillator. Therefore, it would have been obvious to one skilled in the art at the time of the invention to modify Saeki's first delay line to include the odd number of inverters for the purpose of having a ring oscillator in the clock recovery circuit.

Allowable Subject Matter

8. Claims 22 and 23 would be allowable if rewritten or amended to overcome the claim objections, set forth in this Office action.

9. Claims 9,17 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and overcome the claim objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Ahn whose telephone number is (571) 272-3044. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sam K. Ahn
11/3/05

YOUNG T. TSE
PRIMARY EXAMINER